IN THE CLAIMS:

Please amend the claims as follows. For the convenience of the Examiner, all pending claims, whether amended or not, are presented.

Claims 1-7 (Canceled)

8. (Original) A method for identifying false paths, comprising:
providing a path corresponding to a circuit design;
determining whether a set of final value conditions are satisfied;
determining whether a set of side value propagation conditions are satisfied;
determining whether a set of initial value conditions are satisfied;
determining whether the path is false based on at least one of the set of final value conditions, the set of side value propagation conditions, and the set of initial value conditions.

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9. (Currently Amended) The method of claim 8, further comprising:
determining whether a set of slower path conditions are satisfied, and
wherein determining whether the path is false is based on at least one of the set of final value conditions, the set of side value propagation conditions, ~~and~~ the set of initial value conditions, and the set of slower path conditions.

10. (Original) The method of claim 8, wherein the set of final value conditions and the set of side value propagation conditions correspond to a first time frame and the set of initial value conditions corresponds to a second time frame, different from the first time frame.

11. (Currently Amended) ~~The method of claim 8, further~~ A method for identifying false paths, comprising:

providing a first set of paths corresponding to the circuit design, the first set of paths having single-path ~~components~~ component logic blocks and multiple-path ~~components~~ component logic blocks; ~~and~~

extracting a second set of paths from the first set of paths, the second set of paths having no multiple-path ~~components~~ component logic blocks; ~~and~~

providing a path corresponding to a circuit design by selecting the path from the second set of paths;

determining whether a set of final value conditions are satisfied;

determining whether a set of side value propagation conditions are satisfied;

determining whether a set of initial value conditions are satisfied; and

determining whether the path is false based on at least one of the set of final value conditions, the set of side value propagation conditions, and the set of initial value conditions.

12. (Original) The method of claim 8, wherein at least one of determining whether a set of final value conditions are satisfied, determining whether a set of side value propagation conditions are satisfied, and determining whether a set of initial value conditions are satisfied, is performed by an automatic test pattern generation (ATPG) tool.

13. (Currently Amended) A method for false path identification within a circuit design, comprising:

receiving a first set of paths corresponding to the circuit design;

providing a set of conditions corresponding to at least one path of the first set of paths to an automatic test pattern generation (ATPG) tool, the

ATPG tool having an ATPG model corresponding to at least a portion of the circuit design, the set of conditions comprising whether a final value condition is satisfied, whether one or more side value propagation conditions are satisfied, whether an initial value condition is satisfied and whether one or more slower path conditions are satisfied;

the ATPG tool generating a response to the set of conditions using the ATPG model; and

identifying a false path within the first set of paths based on the response from the ATPG tool.

14. (Original) The method of claim 13, further comprising after receiving the first set of paths, translating the first set of paths.

15. (Original) The method of claim 13, further comprising:

after receiving the first set of paths, extracting a second set of paths from the first set of paths, wherein the set of conditions corresponds to at least one path of the second set of paths.

16. (Canceled)

17. (Currently Amended) The method of claim ~~16~~ 13, wherein the response to the set of conditions from the ATPG tool indicates whether the set of conditions is satisfied.

18. (Currently Amended) ~~The method of claim 13,~~ A method for false path identification within a circuit design, comprising:

receiving a first set of paths corresponding to the circuit design from a static analysis tool;

providing a set of conditions corresponding to at least one path of the first set of paths to an automatic test pattern generation (ATPG) tool, the ATPG tool having an ATPG model corresponding to at least a portion of the circuit design;

the ATPG tool generating a response to the set of conditions using the ATPG model; and

identifying a false path within the first set of paths based on the response from the ATPG tool, wherein ~~the~~ a false path report of the false path is fed back to the static analysis tool.

19. (Original) The method of claim 13, wherein the ATPG tool is a commercially available ATPG tool.

20. (Original) The method of claim 13, wherein receiving the first set of paths comprises receiving the first set of paths from a static analysis tool.

21. (Currently Amended) A ~~design analysis tool capable of~~ method for identifying false paths~~, stored via a computer readable medium, said computer readable medium~~ comprising:

~~a first plurality of instructions for receiving~~ determining a ~~path~~ first set of paths corresponding to a circuit design, the first set of paths having single-path component logic blocks and multiple-path component logic blocks;

extracting a second set of paths from the first set of paths, the second set of paths having no multiple-path component logic blocks;

selecting a path from the second set of paths;

~~a second plurality of instructions for~~ determining whether a set of final value conditions are satisfied;

~~a third plurality of instructions for~~ determining whether a set of side value propagation conditions are satisfied;

~~a fourth plurality of instructions for~~ determining whether a set of initial value conditions are satisfied; and

~~a fifth plurality of instructions for~~ determining whether the path is false based on at least one of the set of final value conditions, the set of side value propagation conditions, and the set of initial value conditions.

22. (Currently Amended) The ~~computer readable medium~~ method of claim 21, further comprising:

~~a sixth plurality of instructions for~~ determining whether a set of slower path conditions are satisfied, and ~~wherein the fifth plurality of instructions comprises instructions for~~ determining whether the path is false ~~is~~ based on at least one of the set of final value conditions, the set of side value propagation conditions, ~~and~~ the set of initial value conditions, and the set of slower path conditions.

Claim 23 (Canceled)

24. (Currently Amended) A ~~design analysis tool capable of~~ method for interfacing between a static analysis tool and an automatic test pattern generation (ATPG) tool, capable of identifying false paths within a circuit design, ~~and stored via a computer readable medium, said computer readable medium~~ comprising:

~~a first plurality of instructions for~~ receiving a first set of paths corresponding to the circuit design;

~~a second plurality of instructions for~~ providing a set of conditions corresponding to at least one path of the first set of paths to the ATPG tool, the ATPG tool having an ATPG model corresponding to at least a portion of the circuit design;

~~a third plurality of instructions for~~ receiving a response to the set of conditions generated by the ATPG tool using the ATPG model; and

~~a fourth plurality of instructions for~~ identifying a false path within the first set of paths based on the response from the ATPG tool.

25. (Currently Amended) The ~~computer readable medium~~ method of claim 24, further comprising ~~a fifth plurality of instructions for~~ translating the first set of paths after receiving the first set of paths.

26. (Currently Amended) The ~~computer readable medium~~ method of claim 24, further comprising:

~~a fifth plurality of instructions for~~ extracting a second set of paths from the first set of paths, wherein the set of conditions corresponds to at least one path of the second set of paths.

27. (Currently Amended) The ~~computer readable medium~~ method of claim 24, wherein the set of conditions comprises at least one of final value conditions, initial value conditions, side propagation value conditions, and slower path conditions.

28. (Currently Amended) The ~~computer readable medium~~ method of claim 27, wherein the response to the set of conditions from the ATPG tool indicates whether the set of conditions is satisfied.

29. (Currently Amended) The ~~computer readable medium~~ method of claim 24, further comprising ~~a fifth plurality of instructions for~~ providing ~~the~~ a false path report to the static analysis tool.

30. (Original) The method of claim 24, wherein the ATPG tool is a commercially available ATPG tool.

31. (Currently Amended) The method of claim 24, wherein the first set of paths is received from ~~a~~ the static analysis tool.